Journal of Computer Science and Technology Studies
ISSN: 2709-104X
DOI: 10.32996/jcsts
Journal Homepage: www.al-kindipublisher.com/index.php/jcsts

JCSTS
AL-KINDI CENTER FOR RESEARCH AND DEVELOPMENT

| RESEARCH ARTICLE

Low-Power Design for Test Techniques in Sub-7nm Technologies

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| ABSTRACT

Low-power Design for Test (DFT) techniques have become essential in the advancement of sub-7nm semiconductor technologies. As transistor densities increase and physical dimensions decrease, the challenges of managing power consumption during testing have grown significantly. This article explores critical methods for minimizing power consumption while maintaining comprehensive fault coverage in advanced technology nodes. The convergence of increased design complexity and the imperative to reduce power consumption during testing has spurred the development of specialized approaches including switching activity reduction, strategic clock gating, test partitioning, and adaptive testing techniques. These innovations address the unique challenges posed by sub-7nm technologies while ensuring manufacturability and reliability throughout the testing process.

| KEYWORDS

Power-aware testing, Scan chain partitioning, Transition minimization, Multi-voltage domains, Thermal management

| ARTICLE INFORMATION

ACCEPTED: 20 May 2025 **PUBLISHED:** 10 June 2025 **DOI:** 10.32996/jcsts.2025.7.5.107

1. Introduction

Integrated circuits at sub-7nm process nodes have revolutionized modern computing by enabling higher performance, greater transistor density, and improved energy efficiency. The stacked nanosheet gate-all-around transistor architecture presented by Loubet et al. has been instrumental in enabling scaling beyond FinFET technology, allowing for continued dimensional scaling with improved electrostatics and providing a path toward sub-7nm nodes [1]. This technological advancement has resulted in enhanced performance while maintaining power efficiency through better control of short-channel effects.

However, the accompanying increase in power density and testing complexity poses significant challenges for design and manufacturing. Testing during IC production often accounts for a significant portion of overall power consumption, prompting the need for **low-power DFT** techniques. As outlined by Yiming Li et al., power consumption during test can be significantly higher than during normal operation due to several factors including elevated switching activity, reduced correlation between test patterns, and simultaneous activation of multiple design blocks that would normally operate independently [2]. These elevated power conditions can potentially lead to yield loss caused by noise phenomena such as IR-drop and ground bounce, which result in good dies failing tests and being incorrectly discarded.

These methodologies not only ensure comprehensive fault coverage but also prevent over-stressing the chip during testing, which can lead to thermal and reliability issues. Excessive power dissipation during test can cause structural damage to the circuit, including phenomena such as electromigration, hot carrier effects, and oxide breakdown [2]. By implementing specialized scan techniques that consider both test coverage and power constraints, manufacturers can maintain the reliability of modern ICs throughout their lifecycle while ensuring manufacturing defects are properly detected.

2. Challenges in Testing Sub-7nm Technologies

2.1. Power Density Challenges

Higher transistor density in sub-7nm technologies inevitably results in greater power density, making traditional testing methods power-intensive and thermally challenging. As demonstrated by Yiming Li et al., the power consumption during test can be significantly higher than during normal functional operation, with scan testing causing up to 3-5 times more power dissipation [3]. This excessive power consumption is primarily caused by the substantially higher switching activity during scan shifting operations compared to functional operation. In particular, the shift operation in scan testing causes approximately 15-20% of flip-flops to switch states in each clock cycle, compared to only 2-5% during normal operation. According to experimental results on industrial designs, a single transition fault test can consume up to 30% more peak power than the circuit's specified maximum operational power, creating severe thermal challenges that can compromise test reliability.

2.2. Defect Susceptibility and Variability

Sub-7nm nodes are more susceptible to defects arising from variability, requiring sophisticated fault models and extensive test coverage. With physical gate lengths approaching 10-20nm, process variations have more pronounced effects on transistor performance. Pant et al. noted that these variations lead to a wider distribution of delay defects, necessitating more comprehensive test approaches [3]. In experimental data from advanced technology nodes, small delay defects that affect circuit timing by less than 10% of the clock period have been shown to increase by approximately 35% when moving from 10nm to 7nm nodes, requiring more sophisticated delay testing methodologies.

2.3. Testing Complexity and Escaping Defects

As testing complexity grows, undetected faults (test escapes) can lead to catastrophic field failures, necessitating robust DFT strategies. Abadir et al. demonstrated that for a typical SoC design at advanced nodes, approximately 70-80% of transistors need to be covered by scan testing to achieve acceptable quality levels [4]. Their findings indicated that a reduction in fault coverage from 98% to 95% could result in a 2.5× increase in defective parts shipped to customers. This becomes particularly critical in automotive applications where the target defect rate is often below 1 defective part per million (DPM), requiring test coverage exceeding 99% for critical functions.

2.4. Reliability Degradation from Test-Induced Stress

Prolonged testing under high power consumption conditions can cause hotspots and degrade device reliability. Wu et al. observed that thermal cycling during extended test sequences can generate temperature gradients exceeding 15°C across a die [4]. Their analysis found that scan test procedures that repeatedly stress circuits near maximum power can accelerate aging mechanisms, particularly negative bias temperature instability (NBTI), with measurements showing up to 8% degradation in threshold voltage after extended testing periods. This degradation is especially concerning for sub-7nm nodes where operating margins are already constrained, potentially reducing the useful lifetime of devices by 10-15% if power is not properly managed during testing.

Test Parameter	Functional Mode	Test Mode	Technology Node
Power Dissipation (Relative)	1.0	3.0-5.0	Sub-7nm
Flip-Flop Switching Rate	2-5%	15-20%	
Peak Power vs. Specification	100%	130%	
Small Delay Defect Rate	Base	+35%	7nm vs 10nm
Defective Parts Rate	1× at 98% coverage	2.5× at 95% coverage	Advanced SoC

Temperature Gradient	Nominal	15°C across the die	Sub-7nm
Threshold Voltage Degradation	Minimal	8% after extended test	
Device Lifetime Reduction	0%	10-15%	
Required Scan Test Coverage (Automotive)	99%+	N/A	
Transistor Coverage Requirement	N/A	70-80%	Advanced SoC

Table 1: Power Consumption Comparison Between Test and Functional Modes in Sub-7nm Technologies [3, 4]

3. Power Management During Test

3.1. Peak Power Consumption Challenges

Peak power consumption during test can exceed normal operational power, risking structural damage to the device under test (DUT). According to experimental findings by Yu Huang et al., scan-based testing can induce switching activity rates up to 40% higher than during functional operation [5]. Their research on industrial circuits demonstrated that during launch-to-capture cycles in transition fault testing, instantaneous current demands can spike to levels 2-3 times higher than the circuit's specified maximum operational current. This excessive current draw is attributed to the loss of spatial and temporal correlation between test vectors. For a benchmark circuit with 12,000 gates, the researchers observed that while functional operation typically activated 15-20% of the circuit simultaneously, test patterns activated 35-40%, creating power conditions that exceeded design specifications. These conditions can lead to premature electromigration in metal interconnects and accelerated oxide breakdown in gate dielectrics, potentially causing permanent damage to otherwise functional devices.

3.2. Thermal Stress and Aging Effects

Average power dissipation during extended test sequences can cause thermal stress and accelerate aging mechanisms in nanoscale structures. Saxena et al. documented that sustained elevated power consumption during extended test sequences can create junction temperatures 15-25°C above normal operating conditions [5]. Their thermal simulations showed that for every 10°C increase in operating temperature, electromigration rates approximately double, while time-dependent dielectric breakdown (TDDB) acceleration factors range from 1.5 to 2.0. Measurements on test chips revealed that applying 10,000 test vectors at elevated power levels generated thermal cycling equivalent to approximately 100 hours of normal operation, potentially reducing device lifetime by 2-5% through accelerated aging mechanisms. This becomes particularly critical for sub-7nm technologies where operating margins are already constrained and reliability concerns are heightened due to reduced physical dimensions.

3.3. Power Supply Noise Management

Power supply noise resulting from simultaneous switching during scan tests can lead to false failures, necessitating specialized control techniques. Research by P. Rosinger, B.M. Al-Hashimi and K. Chakrabarty demonstrated that simultaneous switching noise during scan operations can induce voltage fluctuations of 10-15% in the power distribution network [6]. Their measurements on a 90nm test chip showed IR-drop magnitudes during scan testing exceeding functional mode drops by factors of 2.1-2.8×. These voltage variations were observed to cause timing violations in up to 7.4% of paths during at-speed testing despite the circuits being functionally sound. The researchers found that by implementing clock gating techniques during scan operations, they could reduce peak power consumption by 34-62% and decrease the false failure rate from 7.4% to 2.1%. Further improvements were achieved using vector-specific power control methods, which reduced maximum instantaneous power by an additional 22% while maintaining the same fault coverage, demonstrating the effectiveness of power-aware test techniques in preserving test quality while minimizing power-related issues.

Parameter	Functional Mode	Test Mode	Technology/Circuit
Switching Activity Rate	Base	+40%	Industrial circuits
Instantaneous Current	1×	2-3×	Industrial circuits
Circuit Activation	15-20%	35-40%	12,000 gate benchmark
Junction Temperature Increase	0°C	15-25°C	Test chips
Electromigration Rate per 10°C	1×	2×	Nanoscale structures
TDDB Acceleration Factor	1×	1.5-2.0×	Nanoscale structures
Aging Equivalence (10,000 vectors)	N/A	100 hours of operation	Test chips
Voltage Fluctuations	Baseline	10-15%	Power distribution network
IR-Drop Magnitude	1×	2.1-2.8×	90nm test chip

Table 2: Test-Induced Power Effects and Mitigation Techniques in Advanced Technologies [5, 6]

4. Scan-Based Low-Power Techniques

4.1. Scan Chain Partitioning and Segmentation

Scan chain partitioning and segmentation enable selective activation of circuit portions during testing, significantly reducing power consumption. Y. Zorian and A. Yessayan demonstrated that by dividing scan chains into multiple segments and controlling them individually, power dissipation during test can be reduced substantially without compromising test quality [7]. Their research implemented a segment-selection technique that achieved up to 67% reduction in average power and 61% reduction in peak power during test application. The approach involved dividing the conventional scan architecture into multiple segments with independent clock control, allowing only one segment to be active during shift operations. For a benchmark circuit with approximately 10,000 scan cells, implementing just four scan segments reduced power consumption by 62.5% with only a 3% increase in overall test application time. The researchers noted that the segment-selection technique required minimal additional hardware overhead, estimated at less than 2% of the total scan architecture area, making it highly practical for implementation in power-constrained designs.

4.2. Scan Cell Reordering for Reduced Switching

Scan cell reordering minimizes transitions between adjacent flip-flops, reducing switching activity during scan shifts. According to Y. Zorian and A. Yessayan strategic arrangement of scan cells can reduce the switching activity during both shift and capture operations by leveraging the correlation between functionally connected flip-flops [7]. Their experimental results on ISCAS

benchmark circuits showed that scan cell reordering achieved power reductions ranging from 23% to 46% during shift operations compared to random ordering. The technique works by analyzing the probability of transitions between flip-flops and positioning those with similar values adjacent to each other in the scan chain. Importantly, this approach incurred zero hardware overhead and could be implemented purely through CAD tools during the design phase, making it an extremely cost-effective technique for power reduction during test.

4.3. Multi-Voltage Domain Testing

Multi-voltage domain testing approaches allow critical sections to be tested at nominal voltages while less critical areas operate at reduced power levels. Research by Bin Zhou and Xinchun Wu demonstrated that applying adaptive voltage scaling during test significantly reduces power consumption without compromising fault coverage [8]. Their experimental data showed that by operating non-timing-critical blocks at reduced voltages during test, overall test power consumption was reduced by up to 55.3%. For a 28nm multicore design with three distinct voltage domains, their approach achieved a 46.7% reduction in energy consumption by testing each domain at its minimum operational voltage while maintaining 100% stuck-at fault coverage. The researchers observed that for paths with timing slack exceeding 30% of the clock period, supply voltage could be reduced by 200mV while still detecting all targeted delay faults. This approach proved particularly effective for sub-10nm designs where power density challenges are most severe, allowing test power consumption to remain within 20% of functional power limits while maintaining comprehensive fault coverage.

5. Advanced Low-Power DFT Methodologies

5.1. Switching Activity Reduction

Reducing switching activity during testing is critical for minimizing dynamic power consumption. V.R. Devanathan, C.P. Ravikumar and V. Kamakoti have demonstrated that filling don't-care bits in test patterns with values that minimize transitions can significantly reduce test power while maintaining fault coverage [9]. Their X-filling technique achieved power reductions of up to 55% compared to random fill methods by targeting low transition weight (TWs) in both shift and capture operations. Experiments on ISCAS benchmark circuits revealed that adjacent filling techniques reduced average test power by 42.1% during scan shift and 38.5% during capture cycles. For a design with 4,802 scan cells, the weighted transition metric during shift operations decreased from 2,105 to 911 after optimization, demonstrating the effectiveness of transition-minimized pattern generation. Their approach maintained 100% stuck-at fault coverage while reducing power consumption, proving that test quality need not be sacrificed for power savings.

5.2. Strategic Clock Gating Implementation

Leveraging clock gating techniques disables inactive portions of the circuit during testing, significantly reducing dynamic power usage. According to V.R. Devanathan, C.P. Ravikumar and V. Kamakoti clock gating strategies can be particularly effective when combined with scan chain partitioning [9]. Their evaluation showed that applying clock gating to inactive scan segments reduced shift power by up to 74% with only a 2.3% increase in test application time. In their experiments on industrial designs, activating only one out of four scan segments during shift operations reduced switching activity by 76.1% with minimal area overhead (approximately 1.8% of scan architecture). This approach maintains full structural fault coverage while dramatically reducing dynamic power consumption during test, making it particularly suitable for designs already incorporating functional clock gating for low-power operation.

5.3. Independent Partition Testing

Breaking the design into smaller, independently testable partitions lowers instantaneous power demands by testing one section at a time. P. Basker and A. Arulmurugan demonstrated that dividing a system into independently testable partitions based on power analysis can reduce test power by 35-50% [10]. Their technique applies a systematic partition scheduling approach to minimize power overlap while optimizing test time. For a complex SoC containing eight major functional blocks, their power-aware test scheduling reduced peak power consumption from 1.85W to 0.82W with only a 12% increase in total test time. Thermal simulations showed that the maximum die temperature during test decreased from 112°C to 86°C, eliminating previously observed thermal-induced test failures while maintaining comprehensive fault coverage.

5.4. Low-Power BIST Architectures

Advances in low-power BIST architecture include techniques for reducing test pattern generation and compression overheads. Research by P. Basker and A. Arulmurugan has shown that enhanced BIST controllers incorporating low-power pattern generation can achieve up to 64% power reduction compared to conventional LFSR-based approaches [10]. Their LP-LFSR architecture demonstrated an average power reduction of 57.2% across benchmark circuits while maintaining equivalent fault coverage. Implementation on a 45nm design showed that the low-power BIST architecture increased gate count by only 2.1% while reducing test power by 61.3%, making it an excellent trade-off for power-constrained applications.

5.5. Adaptive Testing Implementation

Adaptive testing techniques dynamically adjust parameters such as clock speed and voltage based on thermal and power conditions during testing. According to P. Basker and A. Arulmurugan, closed-loop adaptive testing systems can reduce test energy by 40-52% by selecting optimal parameters based on real-time monitoring [10]. Their implementation uses on-chip temperature sensors to maintain thermal conditions within safe operating limits by dynamically adjusting test clock frequencies between predetermined levels. Experimental results showed that with just five discrete frequency steps between 500MHz and 1.2GHz, the adaptive system reduced average test energy by a factor of 2.1× while ensuring maximum temperature remained below 95°C, preventing thermal shutdown during test while maintaining required fault coverage levels.

DFT Technique	Power Reduction	Performance Impact	Implementation Overhead	Benchmark/Reference Circuit
X-Filling Technique	55%	No impact on fault coverage	Minimal	ISCAS benchmark circuits
Adjacent Filling - Scan Shift	42.1%	100% stuck-at fault coverage	Minimal	ISCAS benchmark circuits
Adjacent Filling - Capture Cycle	38.5%	100% stuck-at fault coverage	Minimal	ISCAS benchmark circuits
Transition Weight Optimization	56.7% (2,105 to 911)	No impact	Minimal	4,802 scan cell design
Clock Gating with Scan Partitioning	74%	2.3% increase in test time	1.8% area overhead	Industrial designs
Segment Activation (1 of 4)	76.1%	No coverage impact	1.8% area overhead	Industrial designs
Independent Partition Testing	35-50%	12% increase in test time	Moderate	Complex SoC
Power-Aware Test Scheduling	55.7% (1.85W to 0.82W)	12% increase in test time	Minimal	8-block SoC
Enhanced BIST Controllers	64%	No coverage impact	2.1% gate count increase	LFSR-based approaches
LP-LFSR Architecture	57.2%	Equivalent fault coverage	2.1% gate count increase	Benchmark circuits

DFT Technique	Power Reduction	Performance Impact	Implementation Overhead	Benchmark/Reference Circuit
X-Filling Technique	55%	No impact on fault coverage	Minimal	ISCAS benchmark circuits
Adjacent Filling - Scan Shift	42.1%	100% stuck-at fault coverage	Minimal	ISCAS benchmark circuits
Low-Power BIST Implementation	61.3%	Equivalent coverage	2.1% area overhead	45nm design
Adaptive Testing Systems	40-52%	No coverage impact	Temperature sensors required	Test energy measurement
5-Step Frequency Adaptation	52.4% (2.1× reduction)	Temperature below 95°C	On-chip sensors	500MHz-1.2GHz range

Table 3: Effectiveness Comparison of Low-Power DFT Methodologies for Sub-7nm Technologies [9, 10]

6. Implementation Considerations

6.1. Power-Constrained Test Pattern Generation

Test pattern generation must balance power constraints with fault coverage requirements, often requiring specialized algorithms. Research by P. Basker and A. Arulmurugan demonstrates that incorporating power awareness into test generation can reduce test power consumption by 30-45% without significant impact on fault coverage [11]. Their experimental results on benchmark circuits showed that power-constrained test generation produced patterns with an average of 36.7% lower switching activity compared to conventional ATPG. On the b19 benchmark circuit, their approach achieved a reduction in peak test power from 18.9 units to 8.24 units while maintaining 97.2% fault coverage, an improvement of 56.4% in power efficiency with only a 1.3% reduction in coverage. The researchers found that optimizing don't-care bit filling based on Hamming distance metrics provided an additional 8.3% power reduction, demonstrating the significant impact of intelligent pattern generation on overall test power consumption.

6.2. DFT Area and Performance Impact

DFT insertion impacts overall chip area and performance, necessitating careful trade-off analysis during the design phase. According to data presented by V. Chickermane, B. Foutz and B. Keller, implementing scan chain partitioning and clock gating for low-power testing typically increases overall chip area by 2-4% but can reduce test power by 50-70% [12]. Their analysis of implementation costs across multiple benchmark circuits revealed that dividing scan chains into four segments increased gate count by approximately 3.2% while reducing shift power by 68.3%. For the s38584 benchmark circuit, implementing mutually exclusive scan segment activation required 246 additional gates (representing an overhead of 2.8%) but reduced capture power from 1,843 units to 578 units, a 68.6% improvement. The researchers noted that proper physical design optimization could limit clock skew penalties to less than 5% even with the additional control logic, ensuring minimal impact on functional performance.

6.3. Power Management Infrastructure Integration

Integration with power management infrastructure allows for leveraging existing power control mechanisms during test mode operation. Research by P. Basker and A. Arulmurugan showed that coordinating test operations with system power management can reduce overall implementation costs by 15-25% compared to separate test power control solutions [11]. Their approach to power-constrained test scheduling demonstrated that integrating with existing power control infrastructure eliminated the need for dedicated test power controllers, reducing gate count requirements by an average of 843 gates per power domain. Experimental results on a system with five power domains showed an overall area saving of 4,215 gates (approximately 0.3% of

total chip area) while achieving a 41.8% reduction in test power through coordinated management of domain-specific test operations.

6.4. Test Scheduling Optimization

Test scheduling optimization can further reduce power consumption by avoiding simultaneous high-power test operations. Through experimental validation, V. Chickermane, B. Foutz and B. Keller demonstrated that power-aware test scheduling using graph coloring techniques can reduce peak test power by 25-45% compared to conventional scheduling approaches [12]. Their algorithm for scheduling tests across multiple scan segments achieved a reduction in peak power from 578 units to 321 units for the s38584 benchmark circuit while maintaining the same overall test application time. For designs with multiple clock domains, their technique reduced maximum instantaneous power consumption by 37.5% by optimizing the relative phasing of test operations in different domains. Additionally, their approach for selective activation of mutually exclusive scan segments ensured that only one segment was active during shift operations, effectively distributing power consumption over time and reducing thermal stress without increasing total test application time.

7. *Conclusion*

Low-power DFT techniques represent a critical component in ensuring the viability and reliability of integrated circuits at sub-7nm process nodes. By implementing specialized methodologies such as scan chain partitioning, transition minimization, and adaptive testing, manufacturers can effectively balance the competing requirements of comprehensive fault coverage and thermal management. These techniques not only prevent excessive power consumption during testing but also mitigate potential reliability issues caused by thermal stress and aging effects. As semiconductor technology continues its progression toward even smaller geometries, the development and refinement of power-aware testing strategies will remain essential to maintaining high quality standards while addressing increasingly stringent power constraints in advanced technology nodes.

Funding: This research received no external funding.
Conflicts of Interest: The authors declare no conflict of interest.
Publisher's Note: All claims expressed in this article are solely those of the authors and do not necessarily represent those of their affiliated organizations, or those of the publisher, the editors and the reviewers.

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